Software-Defined Radio (1)

- Consider the techniques seen in previous lectures:
  - Fixed-point optimization
  - Multiplierless filters
  - CORDIC
- These techniques are especially useful when designing dedicated hardware with no programmability or a low-degree of programmability.
- Hardware can operate at relatively low frequencies such as 10 to 20 MHz.
PARALLEL PROCESSING

- Central question:
  - How to increase the performance?

- Increasing the clock frequency:
  - Leads to the generation of too much power, overheating, etc.

- Parallel processing is the solution:
  - Not only for computations
  - Also for data transport, memories, etc.

VECTOR PROCESSING, SIMD

- One way to introduce parallelism without modifying too much a processor’s architecture is to apply the same instruction to the multiple data:
  - Single Instruction Multiple Data (SIMD)
  - Also called: vector processing
  - Think of computations that are repeated on multiple data and are mutually independent:
    - Taps in an FIR filter
    - Butterflies in the same stage of an FFT
    - Etc.

VERY-LARGE-INSTRUCTION WORD: VLIW (1)

- Multiple parallel FUs, possibly different and pipelined
- Load-store architecture:
  - Communication with memory is always via register files.
  - Register files are possibly multi-ported.
- Each FU can receive an instruction every clock cycle
- Each RISC instruction = one issue slot
- No dependencies between different RISC instructions
  - Orthogonal microcode
  - Compiler friendly
- One instruction = many RISC instructions

VLIW (2)

- Example: PHILIPS/NXP TRIMEDIA
  - Assume 128 registers → 7 bits address
  - Long instruction words e.g. (3*7+4)*25=625 bits
  - Many ports on the register file e.g. 75
MULTICORE PROCESSORS

- Chips consist of multiple full-fledged processors.
- Each of these can e.g. be SIMD.
- Threads are often the model of computation.
- A run-time scheduler dispatches threads across the cores
  - Cores may be able to execute multiple threads simultaneously.

COARSE-GRAIN RECONFIGURABLE

- FPGAs are fine-grain reconfigurable:
  - One roughly builds digital systems by connecting bit-level building blocks such as AND and OR gates (actually, by configuring look-up tables and interconnections)
- Coarse-grain reconfigurable architectures have building blocks at the level of ALUs, multipliers, etc.
  - Proper configuration e.g. creates a data-path able to compute an entire FFT butterfly.

DSP FOR SOFTWARE-DEFINED RADIO

- Check the following paper:
- The paper presents several ICs proposed for software-defined radio (SDR):
  - SDR: approach to realize radio functions (mixing, filtering, etc.) on processors.
- Check references in paper to really understand specific solutions.

SDR-PLATFORM CHARACTERISTICS

- Platforms are mixture of generic processors and dedicated co-processors (e.g. for LDPC decoding; LDPC = low-density parity check).
- Often also a mix of SIMD and VLIW.
- Next to DSPs a RISC-style processor is available for overall control and control-dominated parts of the processing.
- Programming such platforms is very complex and quite some effort is spent in compilers and other programming aids.